This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (canceled)

A memory, comprising:

a plurality of memory cells providing at least 256 meg of storage;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

not more than two layers of metal conductors providing interconnection between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 2 (canceled)

The memory of claim 1 wherein said memory is fabricated on a die approximately 24.7 mm by 15 mm.

Claim 3 (canceled)

The memory of claim 1 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 4 (canceled)

The memory of claim 3 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 5 (canceled)

The memory of claim 4 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 6 (canceled)

The memory of claim 5 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said IO lines, said plurality of peripheral devices including a plurality of multiplexors positioned at certain of said intersections of said I/O lines and said datelines for transferring signals on said I/O lines to said datalines.

Claim 7 (canceled)

The memory of claim 6 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 8 (canceled)

The memory of claim 7 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexors responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexors.

Claim 9 (canceled)

The memory of claim 8 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 10 (canceled)

The memory of claim 9 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 11 (canceled)

The memory of claim 3 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 12 (canceled)

The memory of claim 3 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 13 (canceled)

The memory of claim 12 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 14 (canceled)

The memory of claim 1 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 15 (canceled)

The memory of claim 1 wherein said pads are centrally located.

Claim 16 (canceled)

The memory of claim 15 wherein said power supply is positioned proximate to said pads.

Claim 17 (canceled)

The memory of claim 1 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 18 (canceled)

The memory of claim 17 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 19 (canceled)

A memory fabricated on a die, comprising:

a plurality of memory cells providing at least 256 meg of storage;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads, and wherein the die is approximately 24.7 mm by 15 mm.

Claim 20 (canceled)

The memory of claim 1 wherein said layers of metal do not exceed two.

Claim 21 (canceled)

The memory of claim 19 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 22 (canceled)

The memory of claim 21 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 23 (canceled)

The memory of claim 23 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 24 (canceled)

The memory of claim 23 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexors, positioned at certain of said intersections of said I/O lines and said datalines for transferring signals on said I/O lines to said datalines.

Claim 25 (canceled)

The memory of claim 24 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a-plurality of-data output buffers -responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 26 (canceled)

The memory of claim 25 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 27 (canceled)

The memory of claim 26 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 28 (canceled)

The memory of claim 27 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 29 (canceled)

The memory of claim 21 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 30 (canceled)

The memory of claim 21 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 31 (canceled)

The memory of claim 30 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 32 (canceled)

The memory such that of claim 19 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 33 (canceled)

The memory of claim 19 wherein said pads are centrally located.

Claim 34 (canceled)

The memory of claim 33 wherein said power supply is positioned proximate to said pads.

Claim 35 (canceled)

The memory of claim 19 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 36 (canceled)

The memory of claim 35 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 37 (canceled)

A memory, comprising:

a plurality of memory cells providing at least 256 meg of storage, said memory calls being fabricated at a density of 791,350 bits per square mil;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 38 (canceled)

The memory of claim 37 wherein said layers of metal do not exceed two.

Claim 39 (canceled)

The memory of claim 37 wherein said memory is fabricated on a die approximately 24.7 mm by 15 mm.

Claim 40 (canceled)

The memory of claim 37 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 41 (canceled)

The memory of claim 40 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 42 (canceled)

The memory of claim 41 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 43 (canceled)

The memory of claim 42 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers, positioned at certain of said intersections of said I/O lines and said data lines for transferring signals on said I/O lines to said data lines.

Claim 44 (canceled)

The memory of claim 43 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 45 (canceled)

The memory of claim 44 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 46 (canceled)

The memory of claim 45 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 47 (canceled)

The dynamic random access memory of claim 46 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 48 (canceled)

The memory of claim 40 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 49 (canceled)

The memory of claim 40 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 50 (canceled)

The memory of claim 49 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 51 (canceled)

The memory of claim 37 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 52 (canceled)

The memory of claim 37 wherein said pads are centrally located.

Claim 53 (canceled)

The memory of claim 52 wherein said power supply is positioned proximate to said pads.

Claim 54 (canceled)

The memory of claim 37 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 55 (canceled)

The memory of claim 54 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 56 (canceled)

A die carrying a 256 meg memory device, said die having not more than two layers of metal conductors.

Claim 57 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of pads located centrally with respect to said array blocks;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies located proximate said plurality of pads for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said plurality of peripheral devices.

Claim 58 (canceled)

A power distribution bus for a memory device constructed of memory blocks organized into an array, said bus comprised of a first plurality of conductors for carrying the voltages used by the array and forming a web surrounding each of the blocks of the array, and a second plurality of conductors extending from said web into each of the memory blocks to form a grid within each of the memory blocks.

Claim 59 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and wherein said power amplifiers are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 60 (canceled)

A voltage regulator for a dynamic random access memory, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

a plurality of power amplifiers for developing a supply voltage for supplying power to the dynamic random access memory, said power amplifiers being responsive to said reference voltage and having a gain greater than one; and

a control circuit for producing control signals for controlling said plurality of power amplifiers.

Claim 61 (canceled)

A dynamic random access memory, comprising:

an array of memory cells configured in separately controllable array blocks;

a plurality of peripheral devices responsive to external signals for writing data into said array blocks and for reading data out of said array blocks;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and at least one of-said power amplifiers being-associated with each of said array blocks;

a plurality of power distribution switches; and

a power distribution bus for delivering said plurality of supply voltages to said array blocks through said plurality of switches and to said plurality of peripheral devices, and wherein said plurality of peripheral devices includes logic for controlling each of said plurality of switches and for controlling the state of each of said power amplifiers.

Claim 62 (canceled)

A voltage regulator for a dynamic random access memory having an array divided into array blocks, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

multiple power amplifiers for developing a supply voltage, said power amplifiers arranged such that certain of said power amplifiers supply power to certain of the array blocks; and

control circuitry for disabling a power amplifier when the array block associated therewith is disabled.

Claim 63 (canceled)

A power supply for a dynamic random access memory having a plurality of array blocks and a plurality of pads located centrally of the array blocks, said power supply comprising:

a plurality of voltage supplies located proximate to the plurality of pads for producing supply voltages for the plurality of array blocks.

Claim 64 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage pump comprised of a plurality of voltage pump circuits and wherein said voltage pump circuits are organized into a plurality of supply groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 65 (canceled)

A voltage pump for an integrated circuit, comprising:

a plurality of voltage pump circuits operable in response to a clock signal input thereto, said plurality of voltage pump circuits being divided into a plurality of groups for operation in response to an enable signal produced by the integrated circuit in one of separate or concurrent operating modes to achieve predetermined levels of power output;

an oscillator circuit for producing said clock signal; and

a regulator circuit for producing first signals for controlling said oscillator circuit.

Claim 66 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices, one of said plurality of voltage supplies including a voltage generator producing an output voltage;

a voltage detection circuit responsive to said output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication-of-the stability-of-the -voltage generator.

Claim 67 (canceled)

A stability sensor for a voltage generator which utilizes pullup and pulldown currents for regulation purposes, said sensor comprising:

a current source responsive to one of the pullup and pulldown currents for producing a source current indicative of the current;

a resistor for generating a voltage in response to the source current; and

an overcurrent circuit responsive to said voltage for producing a signal indicative of an excessive amount of one of the pullup and pulldown current.

Claim 68 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

a powerup sequence circuit for controlling the powering up of certain of the plurality of voltage supplies in response to the condition of previously powered up voltage supplies.

Claim 69 (canceled)

A powerup circuit for an integrated circuit having a voltage supply responsive to a voltage external to the integrated circuit and generating a feedback signal, said powerup circuit comprising:

a first circuit portion responsive to the external voltage for producing a first output signal indicative of whether the external voltage is above a predetermined value; and

a second circuit portion responsive to said first output signal and the feedback signal for producing a first enable signal to enable the voltage supply.

Claim 70 (previously presented)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

Claim 71 (previously presented)

A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first seed row of memory elements;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent groups of memory elements in response to a second external signal;

reading the test data from the subsequent groups of memory elements; and

comparing the test data read from the subsequent groups of memory elements with the test data written to the first seed row of memory elements.

Claim 72 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into said memory cells and for reading information out of said memory cells, said plurality of peripheral devices including a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks; and

a plurality of voltage supplies for generating a plurality of supply voltages for use by said array blocks and said plurality of peripheral devices, and wherein said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said IO lines, and wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said 110 lines to said datalines.

Claim 73 (canceled)

A data path for a dynamic random access memory having a plurality of data cells organized into rows and columns to form a plurality of individual arrays, the plurality of individual arrays organized into rows and columns to form a plurality of array blocks, with the array blocks organized into a plurality of quadrants, said data path comprising:

a plurality of sense amplifiers positioned between adjacent rows of individual arrays;

a plurality of digitlines extending through each individual array and into said sense amplifiers;

a plurality of I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines;

a plurality of datalines running between adjacent columns of individual arrays to form intersections with said I/O lines;

a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said VO lines to said datalines;

a plurality of I/O blocks each responsive to said datalines from one of said plurality of array quadrants;

a plurality of data read multiplexers responsive to said array I/O blocks;

a plurality of data output buffers responsive to said plurality data read multiplexers;

a plurality of data pad drivers responsive to said plurality of data output buffers for making data read from the cells available at a plurality of pads;

a plurality of data in buffers responsive to data available at the plurality of pads; and

a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 74 (canceled)

An output buffer, comprising:

a plurality of output drive transistors connected in series between a first voltage supply and ground;

an output terminal responsive to said series connected transistors;

a latch for receiving data to be output to said output terminal;

a logic circuit responsive to said latch for controlling said output drive transistors to drive a voltage at said output terminal to one of a high and low potential representing a logic state of the data to be output;

a boot capacitor for supplying additional voltage to certain of said drive transistors;

a holding transistor responsive to said logic circuit for connecting said boot capacitor to a second supply voltage; and

a self-timed circuit path connected across said holding transistor and said boot capacitor.

Claim 75 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into and reading data out of said array of memory cells, said peripheral devices including a plurality of programmable multiplexer cells;

a power supply;

a plurality of pads; and

layers of conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 76 (canceled)

A programmable multiplexer cell for use in a memory device, comprising:

a plurality of input lines;

a plurality of output lines;

a plurality of programmable switches connecting said plurality of input lines to said plurality of output lines through said multiplexer.

Claim 77 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending there through, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines;

a power supply for generating a plurality of supply voltages, said power supply voltages including a plurality of generators for producing a bias voltage for biasing said digitlines, said number of generators being equal to said number of array blocks; and

a power distribution bus for delivering said plurality of supply voltages to said plurality of array blocks and said peripheral devices.

Claim 78 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending therethrough;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines, said peripheral devices including a plurality of sense amplifiers for sensing the signals on said digitlines, said sense amplifiers being controlled by control signals having a greater magnitude than the magnitude of the data signals to be written to said memory cells;

a power supply for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said peripheral devices.

Claim 79 (canceled)

A sense amplifier, comprising:

a digitline for connecting an array to I/O lines;

an equalization switch adjacent the array for equilibrating said digitline;

an n-sense amplifier connected across said digitline;

a p-sense amplifier connected across said digitline;

an isolation switch connected between said n-sense and said p-sense amplifier and said equalization switch for isolating said n-sense and p-sense amplifier from the array; and

a connection switch for connecting said digitline to the I/O line.

Claim 80 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells, said plurality of peripheral devices including a plurality of sense amplifiers;

logic for producing a redundant signal for controlling said plurality of peripheral devices; a power supply;

a plurality of pads; and

not more than a first layer and a second layer of metal conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said logic, said power supply, and said plurality of pads, said redundant signal being routed through said sense amplifiers in said second layer of metal.

Claim 81 (canceled)

The memory of claim 70 wherein said test mode logic is responsive to an all row high test condition.

Claim 82 (canceled)

The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 83 (canceled)

The memory of claim 82 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 84 (canceled)

The memory of claim 83 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 85 (canceled)

The memory of claim 84 wherein said multiplexers are positioned at every second individual array.

Claim 86 (canceled)

The memory of claim 70 wherein said array of memory cells is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 87 (canceled)

The memory of claim 86 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 88 (canceled)

The memory of claim 86 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 89 (canceled)

The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 90 (canceled)

The memory of claim 89 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 91 (canceled)

The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 92 (canceled)

The memory of claim 91 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 93 (canceled)

The memory of claim 91 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 94 (canceled)

The memory of claim 70 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 95 (canceled)

The memory of claim 94 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 96 (canceled)

The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 97 (canceled)

The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 98 (canceled)

The memory of claim 70 wherein said memory provides at least 256 meg of storage.

Claim 99 (canceled)

The memory of claim 98 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 100 (previously presented)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral device; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory cells, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory cells.

Claim 101 (canceled)

The system of claim 100 wherein said test mode logic is responsive to an all row high test condition.

Claim 102 (canceled)

The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 103 (canceled)

The system of claim 102 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 104 (canceled)

The system of claim 103 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 105 (canceled)

The system of claim 104 wherein said multiplexers are positioned at every second individual array.

Claim 106 (canceled)

The system of claim 100 wherein said array of memory cells is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 107 (canceled)

The system of claim 106 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 108 (canceled)

The system of claim 106 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 109 (canceled)

The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 110 (canceled)

The system of claim 109 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 111 (canceled)

The system of claim 110 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 112 (canceled)

The system of claim 111 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 113 (canceled)

The system of claim 111 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

Claim 114 (canceled)

The system of claim 100 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 115 (canceled)

The system of claim 114 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 116 (canceled)

The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 117 (canceled)

The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 118 (canceled)

The system of claim 100 wherein said memory provides at least 256 meg of storage.

Claim 119 (canceled)

The system of claim 118 wherein said array provides more than 256 meg of storage. said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 120 (previously presented)

A combination for use in a memory having an array of memory elements, said combination comprising:

test mode logic for determining whether the memory is in a test mode;

a latching responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements; and

an enable circuit responsive to a second external signal when the memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

Claim 121 (canceled)

The combination of claim 120 wherein said first external signal includes a row address strobe signal.

Claim 122 (canceled)

The combination of claim 120 wherein said second external signal includes a column address strobe signal.

Claim 123 (canceled)

The combination of claim 120 wherein said write enable circuit is responsive to a plurality of changes in state of the second external signal for enabling the latched data to be written to a plurality of groups of memory elements, respectively.

Claim 124 (canceled)

The combination of claim 123 wherein each of said groups of memory elements includes approximately twenty five percent of the memory elements.

Claim 125 (canceled)

The combination of claim 124 wherein said second external signal includes a column address strobe signal.

Claim 126 (previously presented)

A method of writing to a plurality of memory elements, comprising the steps of:

writing known data into a first seed group of memory elements;

latching the data from the first seed group of memory elements in response to a first external signal; and

writing the latched data into a second group of memory elements in response to a second external signal.

Claim 127 (canceled)

The method of claim 126 wherein the first external signal is a row address signal and the second external signal is a column address strobe signal.

Claim 128 (canceled)

The method of claim 126 additionally comprising the steps of writing the latched data into a another group of memory elements each time the second external signal changes states.

Claim 129 (canceled)

The method of claim 128 wherein said first group of memory elements includes a row of memory elements and wherein said second and subsequent groups of memory elements each include approximately twenty five percent of the memory elements.

Claim 130 (canceled)

The method of claim 126 wherein said step of latching the data includes the step of connecting each memory element in the first group to one of a plurality of sense amps.

Claim 131 (canceled)

The method of claim 130 wherein said step of connecting each memory element includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in said first group to one of the sense amps.

Claim 132 (canceled)

The method of claim 131 wherein said step of writing the latched data into a second group of memory elements includes the step of connecting each memory element in the second group to one of the sense amps.

Claim 133 (canceled)

The method of claim 132 wherein said step of connecting each memory element in the second group includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in the second group to one of the sense amps.

Claim 134 (canceled)

The method of claim 71 additionally comprising the steps of:

writing the latched data into a second group of memory elements in response to a change in state of the second external signal;

writing the latched data into a third group of memory elements in response to another change in state of the second external signal; and

writing the latched data into a fourth group of memory elements in response to a further change in state of the second external signal.

Claim 135 (previously presented)

A method of testing a portion of a memory array having a plurality of memory elements formed in a plurality of rows, and wherein said array is arranged in a plurality of memory blocks, said method comprising the steps of:

selecting a memory block for testing;

writing test data into a first seed row of memory elements in the selected memory block;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent pluralities of rows of memory elements in response to a second external signal;

reading the test data from the memory block; and

comparing the test data read from the memory block with the test data written into the first seed row.

Claim 136 (original)

The method of claim 135 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

Claim 137 (canceled)

The method of claim 136 additionally comprising the steps of writing the latched data into another plurality of rows each time the column address strobe signal changes state.

Claim 138 (previously presented)

A method, comprising:

inputting to a solid state device a series of control signals;

inputting to the device a voltage outside the range of voltages used to represent logic signals;

inputting at least one address to the device; and

decoding the address to ascertain test mode information.

Claim 139 (original)

The method of claim 138 wherein the step of inputting the voltage includes the step of inputting a voltage higher than the highest voltage used to represent logic signals in the device.

Claim 140 (original)

The method of claim 138 wherein said step of inputting at least one address to the device is performed while the step of inputting a voltage is being performed.

Claim 141 (original)

The method of claim 140 additionally comprising the step of decoding the address information to ascertain if the test mode information includes instructions to test for the presence of the voltage outside the range of voltages used to represent logic signals in the device.

Claim 142 (original)

A method of placing a solid state device into a mode in which it is capable of receiving test mode information, comprising:

inputting to the device a voltage outside the range of voltages used to represent logic signals;

enabling a detector; and

confirming with said detector the presence of the voltage outside the range of voltages used to represent logic signals.

Claim 143 (previously presented)

A method of inputting test mode information to a solid state device, comprising:

enabling a detector;

inputting to the device a voltage outside the range of voltages used to represent logic signals;

confirming the presence of the voltage outside the range of voltages used to represent logic signals; and

inputting to the device at least one address containing test mode information.

Claim 144 (canceled)

The method of claim 143 wherein said step of enabling a detector is performed by the steps of inputting a first address and a sequence of control signals.

Claim 145 (canceled)

The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

Claim 146 (canceled)

The method of claim 143 additionally comprising the step of inhibiting the device from normal operation while said step of inputting a voltage is performed.

Claim 147 (previously presented)

A method of placing a solid state device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

sequentially inputting at least two addresses to said device, said first address containing information used to confirm the presence of said voltage outside the range of voltages used to represent logic signals, and said second address containing information used to place the device into a test mode.

Claim 148 (canceled)

The method of claim 147 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

Claim 149 (canceled)

The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

Claim 150 (canceled)

The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

Claim 151 (canceled)

The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

Claim 152 (original)

A method of placing a solid state memory device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

applying a specific combination of control signals to enable the receipt of a test enable key;

verifying the test enable key and confirming the presence of the applied voltage;

applying said specific combination of control signals to enable the receipt of at least one test mode key; and

decoding the test mode key to place the device in a test mode.

Claim 153 (canceled)

The method of claim 152 wherein the specific combination of control signals includes the assertion of the write signal followed by the assertion of the column address strobe and row address strobe signals.

Claim 154 (canceled)

The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

Claim 155 (canceled)

The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

Claim 156 (canceled)

The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

Claim 157 (canceled)

The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.

Claim 158 (canceled)

The method of claim 152 wherein said test mode keys are received as address information on column address lines.

Claim 159 (canceled)

The method of claim 152 additionally comprising the steps of performing the test specified by the test mode key and outputting the test results.

Claim 160 (original)

A test logic circuit for a solid state memory device, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit.

Claim 161 (original)

The test logic circuit of claim 160 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

Claim 162 (original)

The test logic circuit of claim 160 additionally comprising a circuit for inhibiting said solid state memory device from normal operations when the device is in a test mode.

Claim 163 (original)

A solid state memory device, comprising:

a plurality of memory cells;

a plurality of peripheral devices for writing information into and reading information out of said memory cells; and

a test logic circuit, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit;

said memory device further comprising circuits, responsive to said decoded test mode keys, for performing tests on at least one of said memory cells and peripheral devices.

Claim 164 (original)

The memory device of claim 163 wherein said test mode enable circuit includes logic for receiving a row address strobe signal (RAS), a write column address strobe before RAS signal, the applied voltage, and certain address information on column address lines and for producing therefrom a latch signal.

Claim 165 (original)

The memory device of claim 164 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

Claim 166 (canceled)

The memory device of claim 165 wherein said test mode reset circuit includes logic for receiving a row address strobe signal (RAS), a column address strobe signal (CAS), a write CAS before RAS signal and for producing therefrom a test mode reset signal and a super voltage test mode reset signal.

Claim 167 (previously presented)

The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 168 (previously presented)

The memory of claim 167 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 169 (previously presented)

The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 170 (previously presented)

The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 171 (previously presented)

The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 172 (previously presented)

The memory of claim 70 wherein said memory provides at least 256 meg of storage.

Claim 173 (previously presented)

The memory of claim 172 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 174 (previously presented)

The method of claim 71 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

Claim 175 (previously presented)

The method of claim 174 wherein writing into subsequent groups of memory elements includes writing into multiple rows in response to each cycle of the column address strobe signal.

Claim 176 (previously presented)

The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 177 (previously presented)

The system of claim 176 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 178 (previously presented)

The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 179 (previously presented)

The system of claim 178 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 180 (previously presented)

The system of claim 179 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 181 (previously presented)

The system of claim 180 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 182 (previously presented)

The system of claim 180 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

Claim 183 (previously presented)

The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 184 (previously presented)

The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 185 (previously presented)

The system of claim 100 wherein said memory provides at least 256 meg of storage.

Claim 186 (previously presented)

The system of claim 185 wherein said array provides more than 256 meg of storage. said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 187 (previously presented)

The combination of claim 120 wherein said first external signal includes a row address strobe signal.

Claim 188 (previously presented)

The combination of claim 120 wherein said second external signal includes a column address strobe signal.

Claim 189 (previously presented)

The method of claim 126 wherein the first external signal is a row address signal and the second external signal is a column address strobe signal.

Claim 190 (previously presented)

The method of claim 189 additionally comprising the step of writing into subsequent groups of memory elements in response to each cycle of the column addresses strobe signal.

Claim 191 (previously presented)

The method of claim 126 wherein said step of latching the data includes the step of connecting each memory element in the first seed group to one of a plurality of sense amps.

Claim 192 (previously presented)

The method of claim 191 wherein said step of connecting each memory element includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in said first seed group to one of the sense amps.

Claim 193 (previously presented)

The method of claim 192 wherein said step of writing the latched data into a second group of memory elements includes the step of connecting each memory element in the second group to one of the sense amps.

Claim 194 (previously presented)

The method of claim 193 wherein said step of connecting each memory element in the second group includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in the second group to one of the sense amps.

Claim 195 (previously presented)

The method of claim 142 wherein the receipt of the sequence of a write enable signal, column address strobe signal and a row address strobe signal enables the detector.

Claim 196 (previously presented)

The method of claim 143 wherein said step of enabling a detector is performed by the step of inputting a sequence of control signals.

Claim 197 (previously presented)

The method of claim 196 wherein said sequence of control signals includes a write enable signal, column address strobe signal and row address strobe signal.

Claim 198 (previously presented)

The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

Claim 199 (previously presented)

The method of claim 143 wherein said step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode.

Claim 200 (previously presented)

The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

Claim 201 (previously presented)

The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

Claim 202 (previously presented)

The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

Claim 203 (previously presented)

The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

Claim 204 (previously presented)

The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

Claim 205 (previously presented)

The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

Claim 206 (previously presented)

The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.

Claim 207 (previously presented)

The method of claim 152 wherein said test mode keys are received as address information on column address lines.

Claim 208 (previously presented)

The method of claim 152 additionally comprising the steps of performing the test specified by the test mode key and outputting the test results.